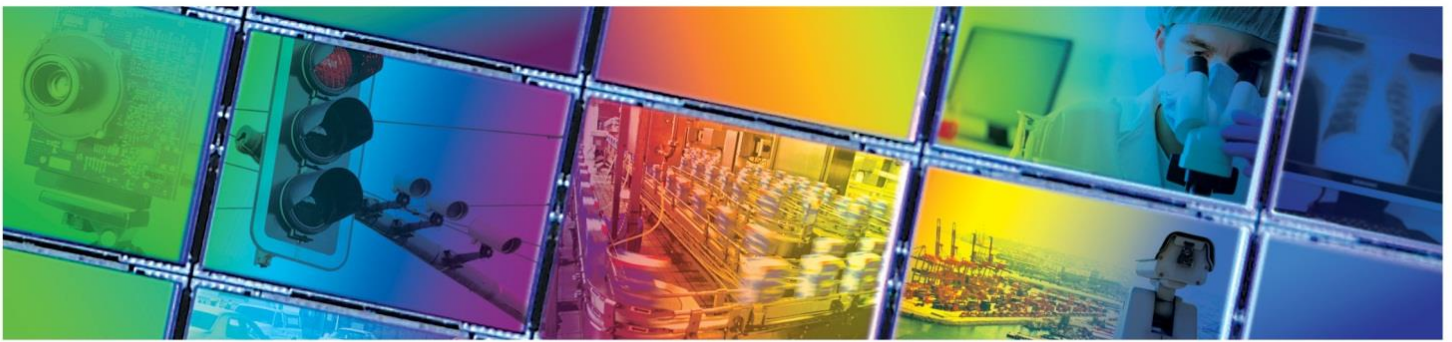


**ON Semiconductor**<sup>®</sup>



**KLI-2104 IMAGE SENSOR**  
**LINEAR CCD IMAGE SENSOR**



**JUNE 12, 2014**  
**DEVICE PERFORMANCE SPECIFICATION**  
**REVISION 1.1 PS-0049**



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## Summary Specification

### KLI-2104 Image Sensor

#### DESCRIPTION

The KLI-2104 Image Sensor is a high dynamic range, multi-spectral, linear solid-state image sensor designed for demanding color scanning applications.

The KLI-2104 contains three parallel linear photodiode arrays, each with 2098 active photosites for the detection of red, green, and blue (R, G, B) signals. A fourth channel, comprised of 4196 pixels, provides high resolution luminance information. This combination allows the KLI-2104 to provide high resolution scans with accurate color reproduction.

The device offers high sensitivity, low noise, and negligible lag.

#### FEATURES

- Quadri-Linear Color Array design (G, R, B, L) for high resolution with accurate color reproduction
- High sensitivity photosites
- Low noise design with negligible image lag
- Pixel-summing support for extended sensitivity and dynamic range
- 5.0 V clock inputs with two-phase register clocking
- Choice of Multi-layer Antireflective Coated (MAR) or Clear Coverglass

#### APPLICATIONS

- Digitization
- Photography



Parameter	Value
Architecture	Quadrilinear CCD
Total Number of Pixels Chroma; Luma	3 x 2222; 1 x 4244
Number of Active Pixels Chroma; Luma	3 x 2098; 1 x 4196
Pixel Size Chroma; Luma	14 μm; 7 μm
Inter-Array Spacing G to R, R to B B to L	84 μm 87.5 μm
Chip Size	35.64 mm (H) x 1.06 mm (V)
Saturation Signal Chroma; Luma	208,000 electrons; 140,000 electrons
Output Sensitivity	12 μV/electron
Peak Quantum Efficiency R; G; B; L	73%; 55%; 62%; 88%
Responsivity R; G; B; L	33; 36; 56; 16 V/μJ/cm <sup>2</sup>
Total Read Noise	30 electrons
Dark Current Chroma; Luma	0.22 pA/pixel; 0.07 pA/pixel
Dynamic Range Chroma; Luma	80 dB; 75 dB
Charge Transfer Efficiency	0.99999
Photoresponse Non-uniformity	15% Peak-Peak
Operating Frequency	20 MHz per output
Package	Ceramic PGA
Cover Glass Options	MAR coated, 2 sides

All parameters are specified at T = 25 °C unless otherwise noted.



## Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0497	KLI- 2104-DAA-EB-AA	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass (no coatings), Standard Grade	KLI-2104 Serial Number
4H0499	KLI- 2104-DAA-EB-AE	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass (no coatings), Engineering Grade	
4H0496	KLI- 2104-DAA-ED-AA	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade	
4H0498	KLI- 2104-DAA-ED-AE	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Grade	

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at [www.truesenseimaging.com](http://www.truesenseimaging.com).

Please address all inquiries and purchase orders to:

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 1964 Lake Avenue  
 Rochester, New York 14615

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 E-mail: [info@truesenseimaging.com](mailto:info@truesenseimaging.com)

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## Device Description

### ARCHITECTURE

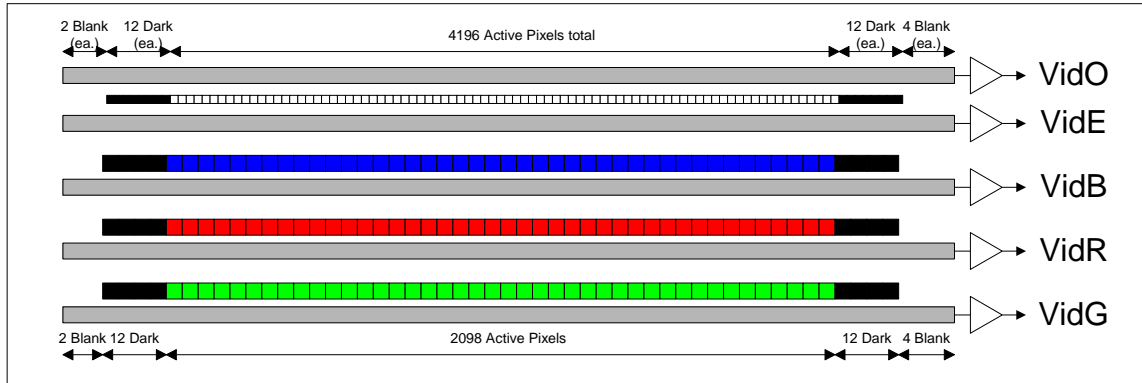


Figure 1: Block Diagram

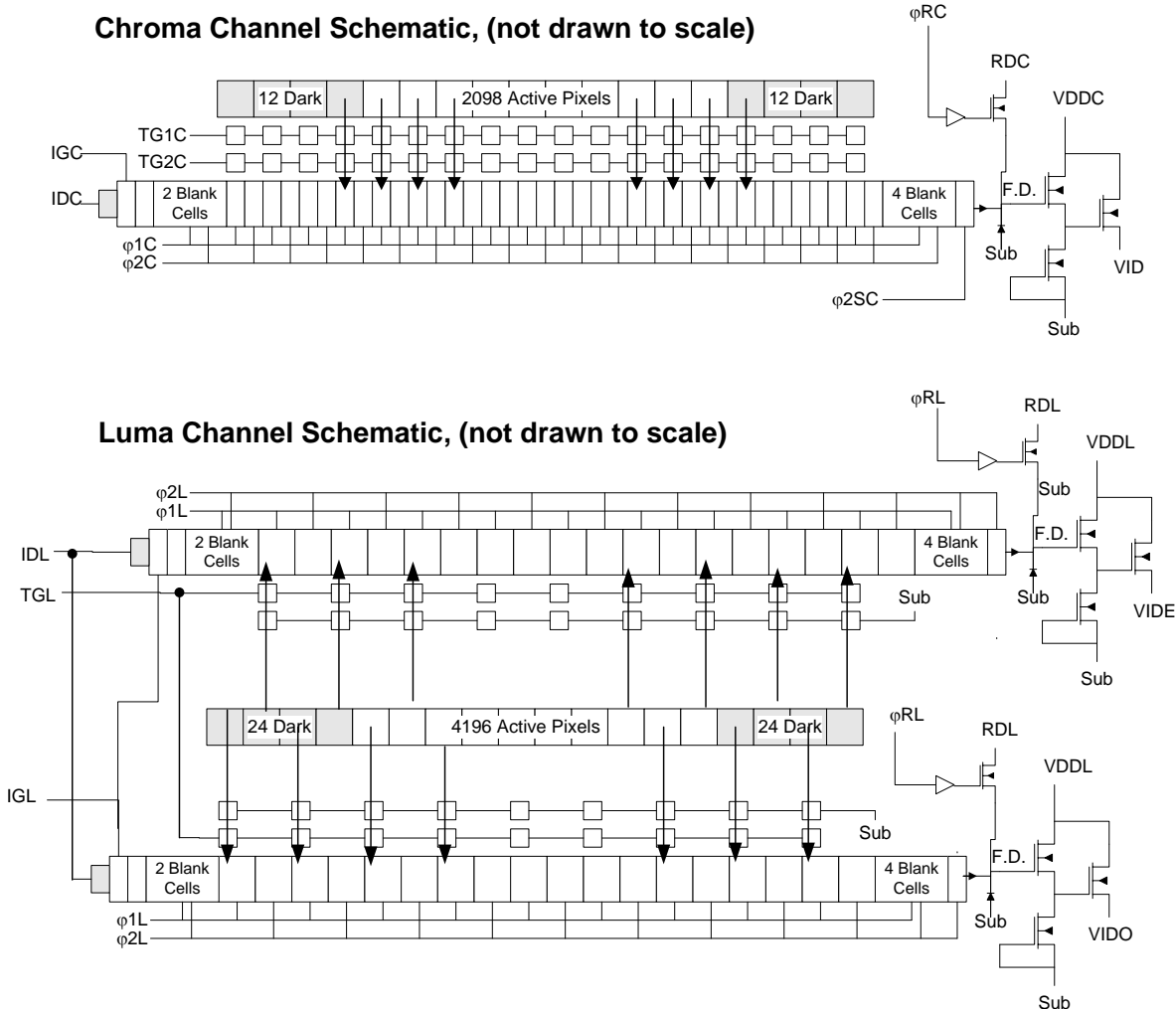


Figure 2: Single Channel Schematic, chroma and luma

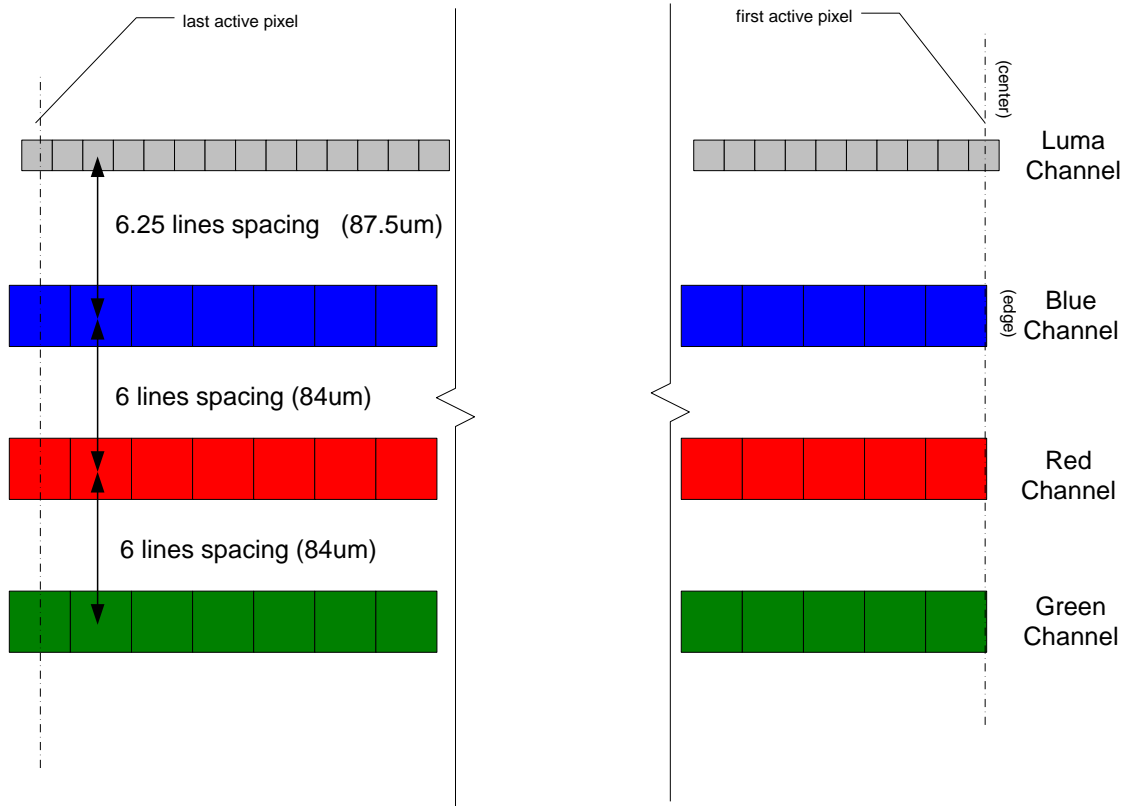


Figure 3: Active Pixel and Channel Alignment – KLI-2104



## IMAGING

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2 for the chroma channels, which are held at a barrier potential. (The luminance channel has only one transfer gate, TG). At the end of the integration period, the CCD register clocking is stopped with the  $\phi 1$  and  $\phi 2$  gates being held in a 'high' and 'low' state respectively. Next, the TG gates are turned 'on' causing the charge to drain from the photodiode into the TG1 storage region. As TG1 is turned back 'off' charge is transferred through TG2 and into the  $\phi 1$  storage region. The TG2 gate is then turned 'off', isolating the shift registers from the accumulation region once again. For the luminance channel, only one TG transfer is required. Complementary clocking of the  $\phi 1$  and  $\phi 2$  phases now resumes for readout of the current line of data while the next line of data is integrated.

## CHARGE TRANSPORT AND SENSING

Readout of the signal charge is accomplished by two-phase, complementary clocking of the  $\phi 1$  and  $\phi 2$  gates. The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (5Vp-p min) clock swings for reduced power dissipation, lower clock noise and simpler driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the  $\phi 2$  clock. Re-settable floating diffusions are used for the charge-to-voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by  $\Delta V_{FD} = \Delta Q / C_{FD}$ , where  $\Delta V_{FD}$  is the change in potential on the floating diffusion,  $\Delta Q$  is the amount of charge, and  $C_{FD}$  is the capacitance of the floating diffusion node. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock,  $\phi R$ .

## PIXEL SUMMING (CHROMA CHANNELS ONLY)

Enabling the pixel - summing feature can vary the effective resolution of the color channels of this sensor. A separate pin is provided for the last shift register gate labeled  $\phi 2SC$ . This gate, when clocked appropriately, stores the summation of signal from adjacent pixels. This combined charge packet is then transferred onto the sense node. As an example, the sensor can be operated in 2-pixel summing mode (1049 pixels), by supplying a clock to  $\phi 2SC$  which is a 75% duty cycle signal at 1/2 the frequency of the  $\phi 2C$  signal, and modifying the  $\phi RC$  clock as depicted in Figure 24. Applications that require full resolution mode (2098 pixels), must tie the  $\phi 2SC$  pin to the  $\phi 2C$  pin. Refer to Figure 23 for additional details.

The luma channel outputs are in an odd and even configuration. The odd pixel value and the even pixel value are available simultaneously during the  $\phi 2$  clock low phase. In this manner, pixel summing is an option off-chip.





## PHYSICAL DESCRIPTION

### Pin Description and Device Orientation

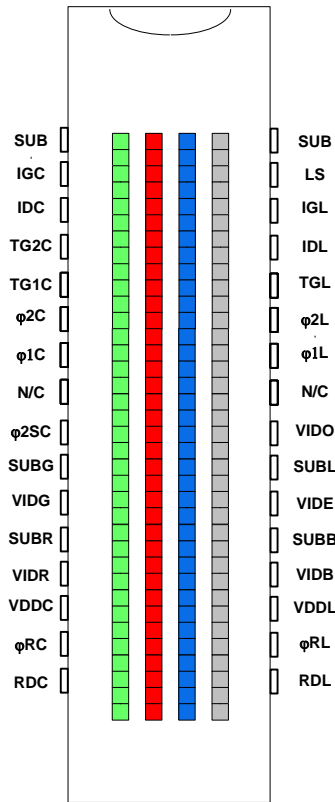


Figure 4: Pinout Diagram

Pin	Name	Description
1	SUB	Substrate / Ground
2	IGC	Test Input - Input Diode, chroma
3	IDC	Test Input - Input Diode, chroma
4	TG2C	Transfer Gate 2 Clock, chroma
5	TG1C	Transfer Gate 1 Clock, chroma
6	φ2C	Phase 2 CCD Clock, chroma
7	φ1C	Phase 1 CCD Clock, chroma
8	N/C	No Connection (Ground)
9	H2SC	Phase 2 Summing Gate, Chroma
10	SUBx	Ground Reference (R,G,B)
11	VIDx	Output Video (R,G,B)
12	SUBx	Ground Reference (R,G,B)
13	VIDx	Output Video (R,G,B)
14	VDDC	Amplifier Supply (chroma)
15	φRC	Reset Clock, chroma
16	RDC	Reset Drain, chroma

Pin	Name	Description
32	SUB	Substrate / Ground
31	LS	Light Shield / Exposure Drain
30	IGL	Test Input - Input Gate, luma
29	IDL	Test Input - Input Diode, luma
28	TGL	Transfer Gate Clock, luma
27	φ2L	Phase 2 CCD Clock, luma
26	φ1L	Phase 1 CCD Clock, luma
25	N/C	No Connection (Ground)
24	VIDO	Output Video (luma odd channel)
23	SUBL	Ground Reference (luma)
22	VIDE	Output Video (luma even channel)
21	SUBx	Ground Reference (R,G,B)
20	VIDx	Output Video (R,G,B)
19	VDDL	Amplifier Supply (luma)
18	φRL	Reset Clock, luma
17	RDL	Reset Drain, luma



## Imaging Performance

Specifications given under nominally specified operating conditions for the given mode of operation at 25 °C,  $f_{CLK} = 1$  MHz, 2.1 msec integration time, MAR coverglass, color filters, and an active load as in the schematic shown in Figure 21 of a typical output bias/buffer circuit, unless otherwise specified. See notes on next page for further descriptions.

Each limit identified as a maximum and/or a minimum is tested and guaranteed for every device. Nominal values are to be considered typical performance values that are design and manufacturing targets. These values are not guaranteed.

## SPECIFICATIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes	Verification Plan <sup>15</sup>
Saturation Output Voltage, Chroma	Vsat, chroma	2.0	2.5	---	Vp-p	1, 9	die
Saturation Output Voltage, Luminance	Vsat, lum	1.2	1.75	---	Vp-p	1, 9	die
Output Sensitivity	$\Delta V_{out}/\Delta N_e$	---	12	---	$\mu V/e^-$		design
Saturation Signal Charge, Chroma	N <sub>e,sat chroma</sub>	---	208,000	---	electrons		design
Saturation Signal Charge, Luminance	N <sub>e,sat lum</sub>	---	146,000	---	electrons		design
Responsivity	R, chroma					2, 9, 10	
Quantum Efficiency	QE, chroma					2, 9, 10	
(Blue channel @ 460 nm)		---	73	---	%	± 10 %	design
(Green channel @ 540 nm)		---	55	---	%	± 10 %	design
(Red channel @ 650 nm)		---	62	---	%	± 10 %	design
(Luma channel @ 550 nm)	QE, luma	---	88	---	%	± 10 %	design
Dynamic Range, chroma	DR, chroma	---	80	---	dB	3	design
Dynamic Range, luma	DR, luma	---	75	---	dB	3	design
Dark Noise, chroma and luma	Noise, dark	---	30	---	electrons		design
Dark Signal Non-Uniformity, chroma	DSNU, chroma	---	2	16	mV p-p	14	die
Dark Signal Non-Uniformity, luma	DSNU, luma	---	2	16	mV p-p	14	die
Dark Current, chroma	I <sub>dark</sub> , chroma	---	0.22	0.5	pA/pixel	4	die
Dark Current, luma	I <sub>dark</sub> , luma	---	0.07	0.2	pA/pixel	4	die
Charge Transfer Efficiency, chroma	CTE, chroma	0.999995	0.999998	1	---	5	die
Charge Transfer Efficiency, luma	CTE, luma	0.999995	0.999998	1	---	5	die
Lag, Chroma	L, chroma	---	0.05	1	%	1st Field	die
Lag, Luma	L, luma	---	0.1	1	%	1st Field	die
DC Output Offset	V <sub>o,dc</sub>	5	6.6	8	Volts	9	die
Photoresponse Non-Uniformity, Low Frequency chroma	PRNUC, Low	---	6	20	% p-p	6	die
Photoresponse Non-Uniformity, Medium Frequency chroma	PRNUC, Med	---	6	20	% p-p	7	die
Photoresponse Non-Uniformity, High Frequency chroma	PRNUC, High	---	3	15	%	8	die
Photoresponse Non-Uniformity, Low Frequency luma	PRNUL, Low	---	6	20	% p-p	6	die
Photoresponse Non-Uniformity, Medium Frequency luma	PRNUL, Med	---	6	20	% p-p	7	die
Photoresponse Non-Uniformity, High Frequency luma	PRNUL, High	---	3	15	%	8	die
Darkfield Defect, brightpoint	Dark Def	---	---	0	Allowed	12	die
Brightfield Defect, dark or bright	Bfld Def	---	---	0	Allowed	13	die
Smear, photodiode to CCD crosstalk	Smear, Chroma						
(Blue channel @ 450 nm)		---	0.2	---	%		design
(Green channel @ 550 nm)		---	0.05	---	%		design
(Red channel @ 650 nm)		---	0.4	---	%		design



Description	Symbol	Minimum	Nominal	Maximum	Units	Notes	Verification Plan <sup>15</sup>
Smear, (Luma channel @ 550 nm)	Smear, Luma	---	1.2	---	%		design
Linearity, maximum from best fit straight line	Linearity, Chroma						
(Blue channel)		---	0.6	---	%		design
(Green channel)		---	1.2	---	%		design
(Red channel)		---	1	---	%		design
(Luma channel)	Linearity, Luma	---	1	---	%		design
DC Amplifier Gain	Gain, DC	---	0.75	---			design
Amplifier Output Resistance	Rout	---	220	---	ohms		design
Output Buffer Bandwidth	f_3dB	---	72	---	MHz		design

Notes:

1. Calculated under a flat field illumination. Defined as the maximum output level achievable before linearity or PRNU performance is degraded beyond specification.
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm. Color filter arrays become transparent after 710 nm. It is recommended that a suitable IR cut filter be used to maintain spectral balance and optimal MTF. See quantum efficiency plots in Figure 6.
3. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between φ1 and φ2 phases must be maintained to minimize clock noise.
4. Dark current doubles approximately every +7 °C.
5. Measured per transfer, 2 phases per pixel. For the typical total line (chroma): (0.99999) 4256 = 0.9583. For the typical total line (luma): (0.99999)4256 = 0.9583. It should be noted that this parameter degrades with increasing horizontal clock frequency.
6. Low frequency response is measured across the entire array with a 1000 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
7. Medium frequency response is measured across the entire array with a 50 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.
8. High frequency response non-uniformity represents individual pixel defects evaluated under a flat field illumination. An individual pixel value may deviate above or below the average response for the entire array by a certain threshold.
9. Increasing the current load (nominally 6 mA) to improve signal bandwidth will decrease these parameters.
10. If resistive loads are used to set current, the amplifier gain will be reduced, thereby reducing the output sensitivity and net responsivity.
11. Where defective pixels are allowed, they will be separated by at least one non-defective pixel within and across channels.
12. Pixels whose response is greater than the average response by the specified threshold, (16 mV). See Figure 5.
13. Pixels, whose response is greater or less than the average response by the specified threshold, contained in the high frequency PRNU specification for that channel. See Figure 5.
14. Absolute difference between the maximum and minimum average signal level for an entire video channel.
15. A "die" parameter is measured on every sensor during production testing. A "design" parameter is quantified during design verification and not guaranteed by specification.

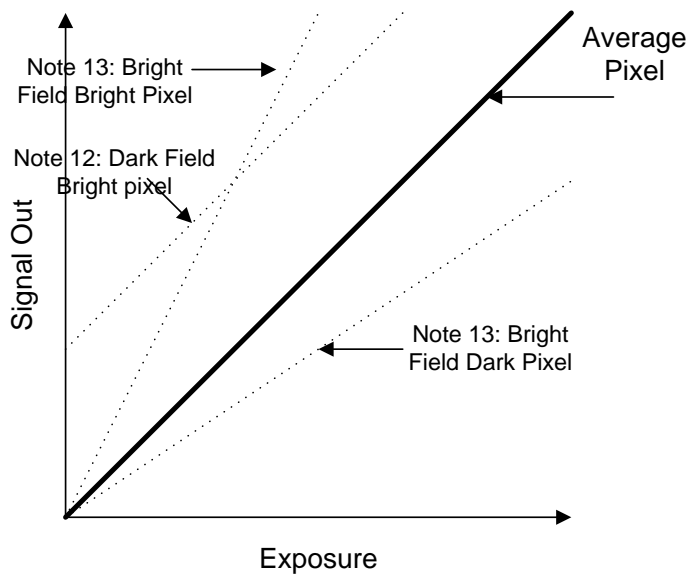


Figure 5: Defective Pixel Classification



### Typical Performance Measures

KLI-2104 Responsivity - Color Channels

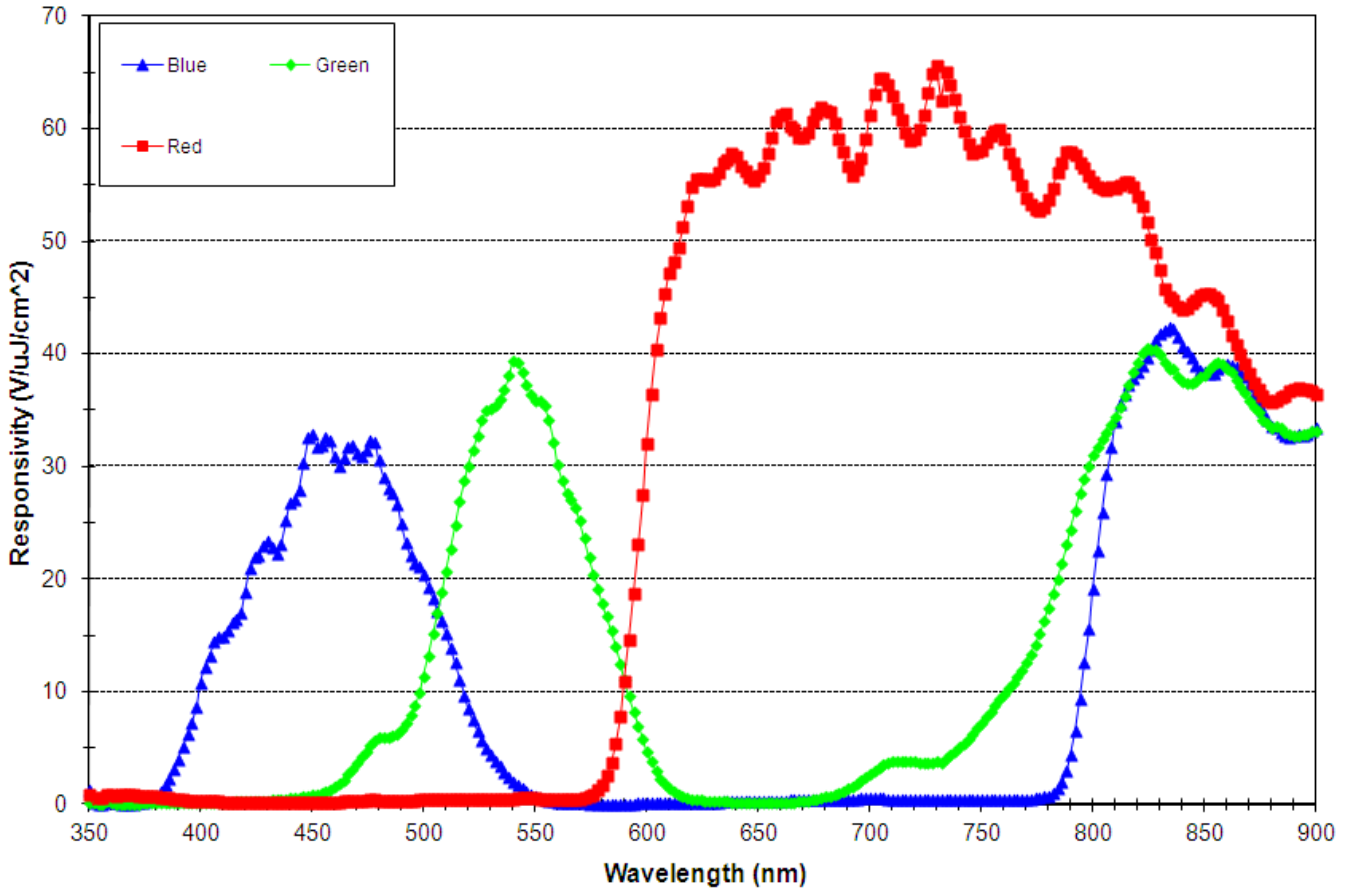


Figure 6: KLI-2104 Responsivity - Color Channels



KLI-2104 Responsivity - Even/Odd Monochrome Channels

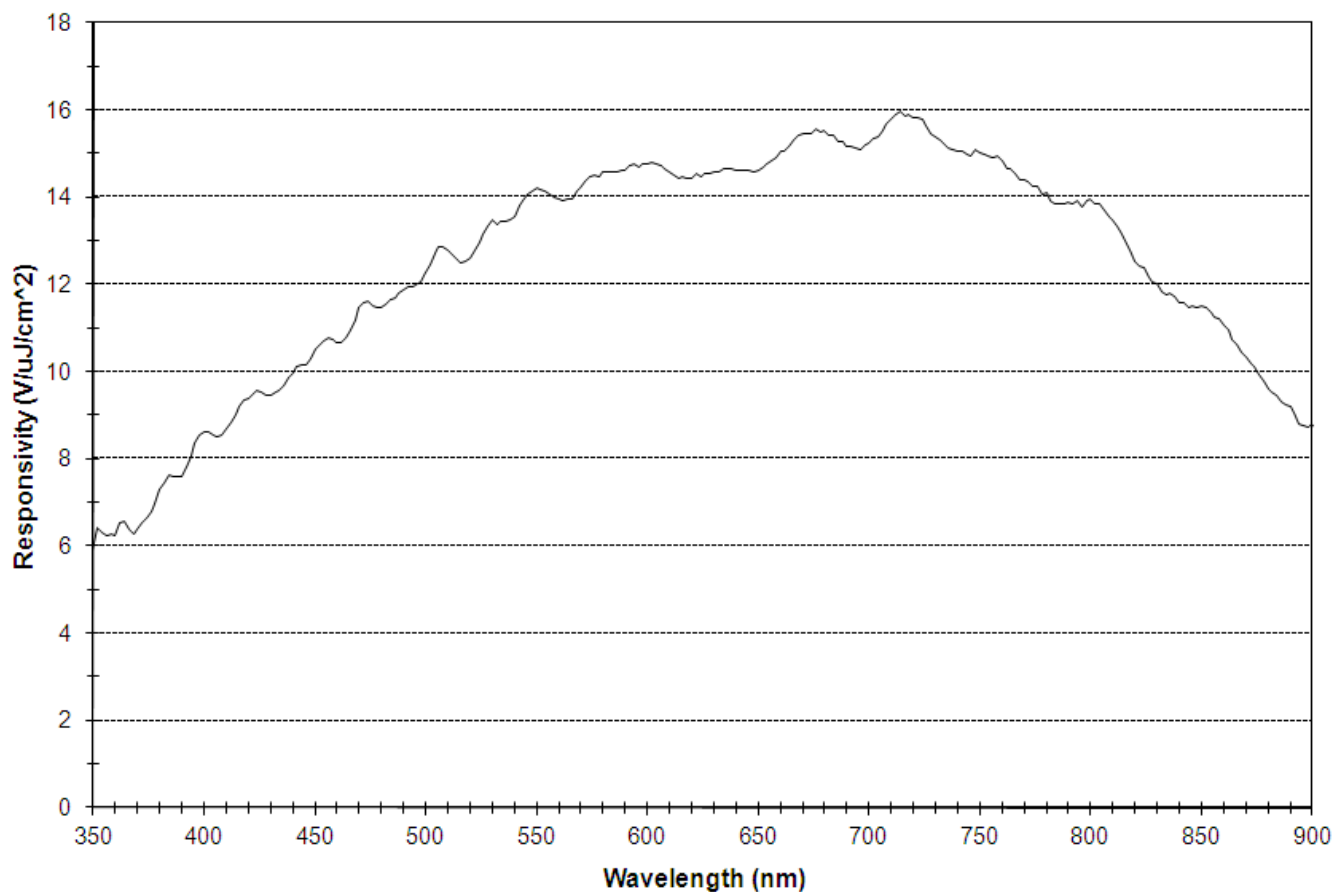


Figure 7: Luminance Channel Responsivity

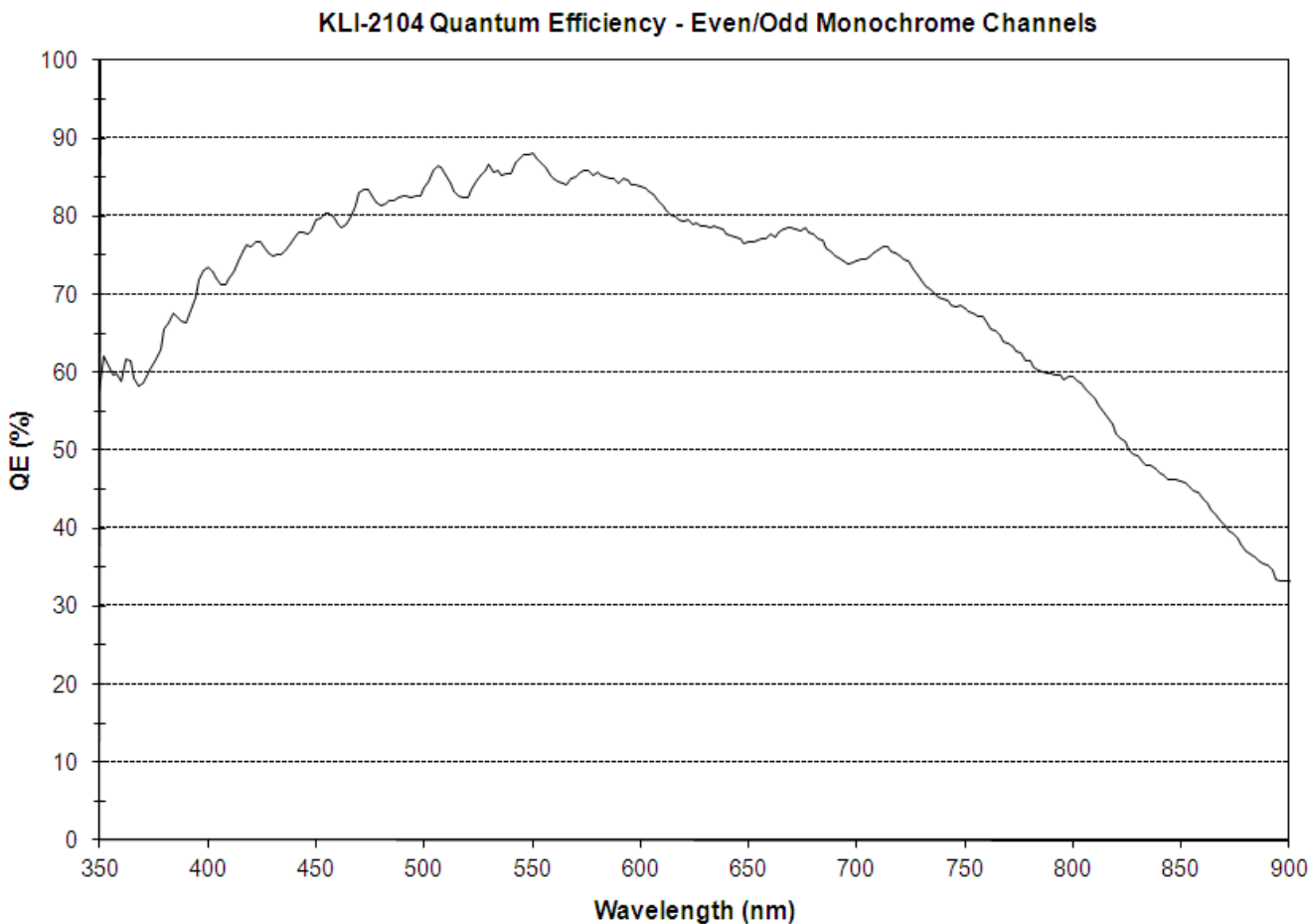


Figure 8: KLI-2104 Quantum Efficiency - Even/Odd Monochrome Channels



KLI-2104 Quantum Efficiency - Color Channels

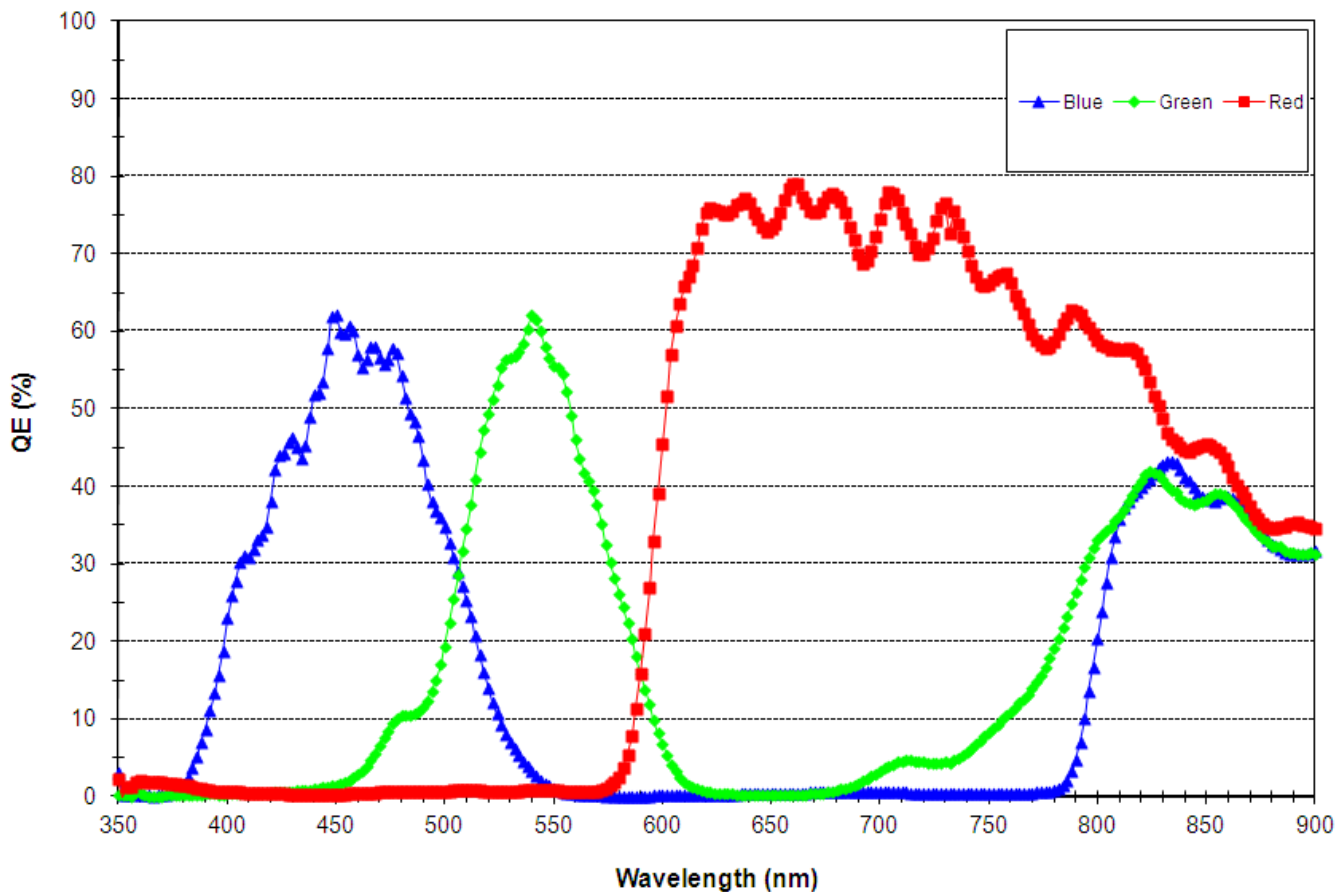


Figure 9: KLI-2104 Quantum Efficiency - Color Channels



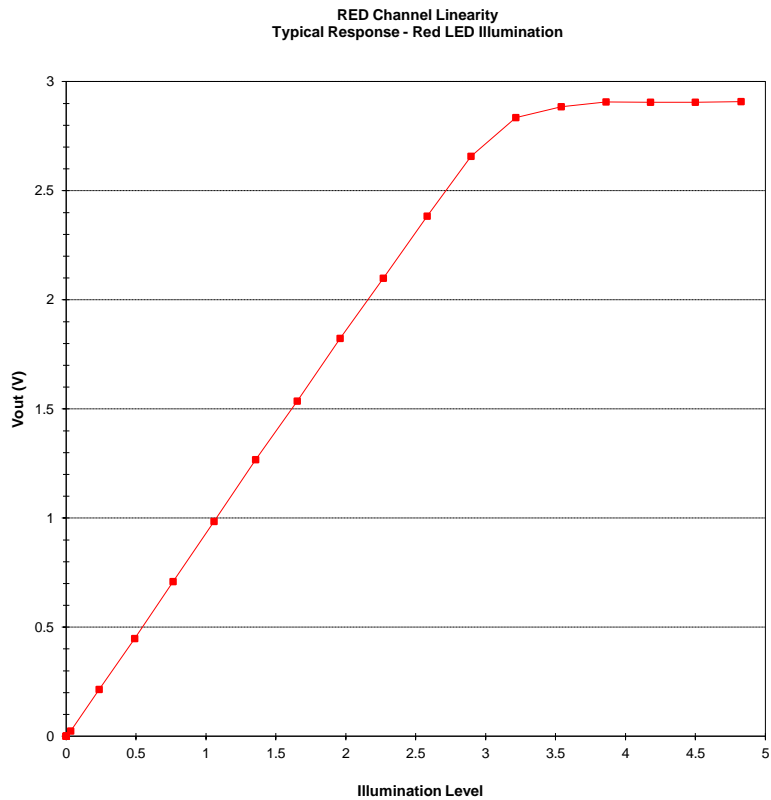


Figure 10: Red Channel Linearity



GREEN Channel Linearity  
Typical Response - Green LED Illumination

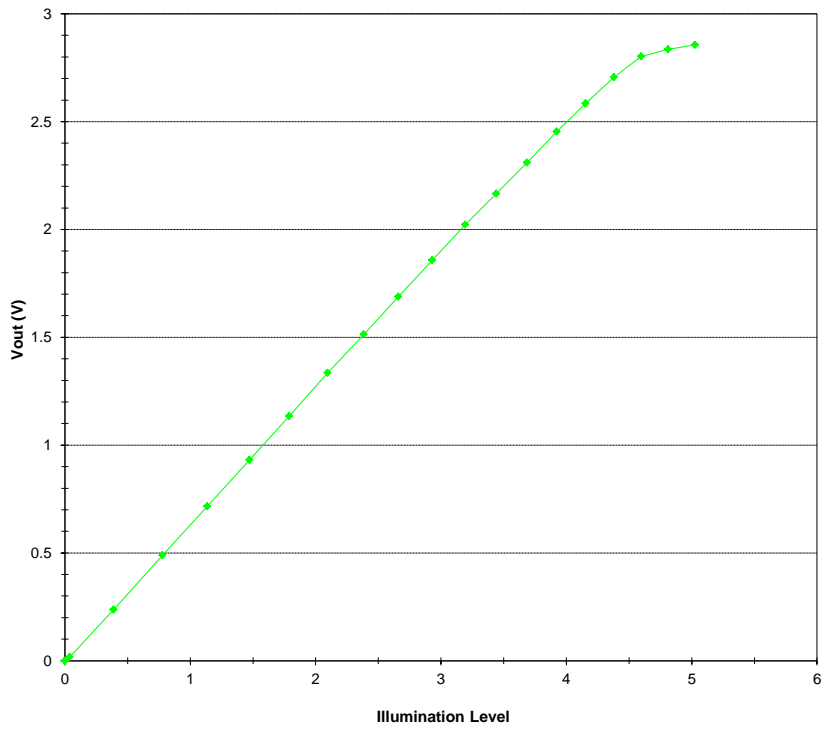


Figure 11: Green Channel Linearity

BLUE Channel Linearity  
Typical Response - Blue LED Illumination

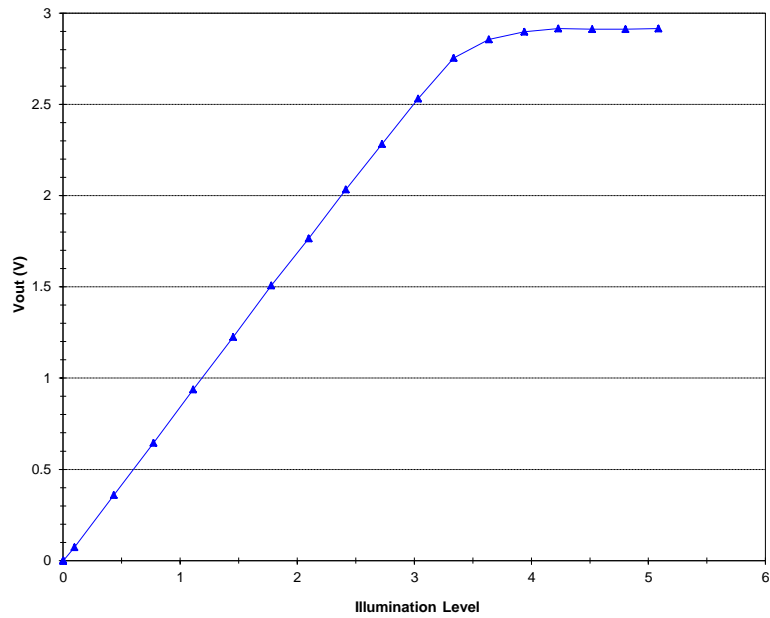


Figure 12: Blue Channel Linearity

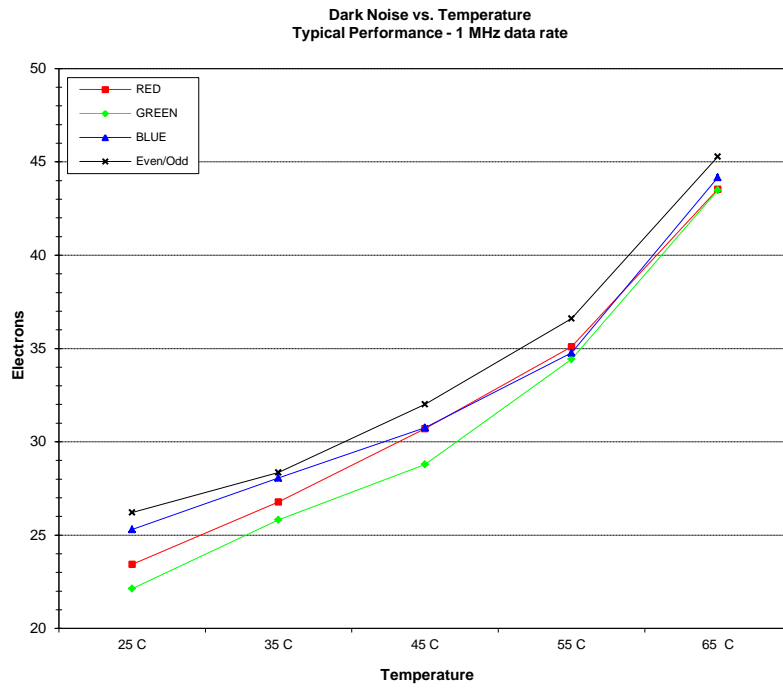


Figure 13: Dark Noise vs. Temperature

**Typical Modulation Transfer Function KLI-2104 Chroma Channels (MTF)**

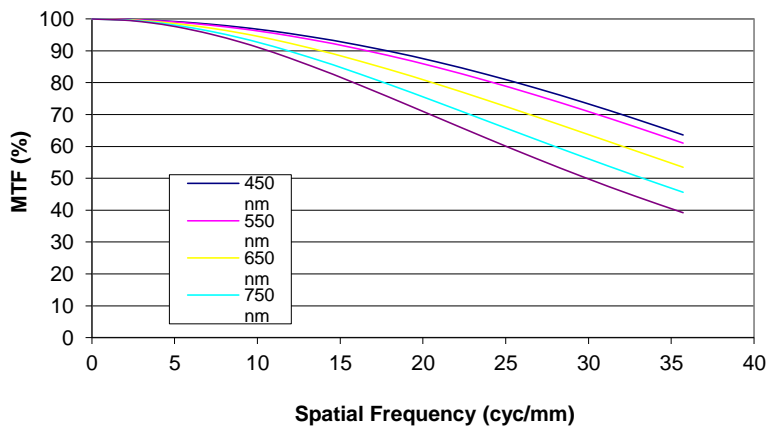


Figure 14: Typical Modulation Transfer



**KLI-2104 Smear (photodiode-to-CCD crosstalk)  
@ 450 nm - 800 nm Typical Performance**

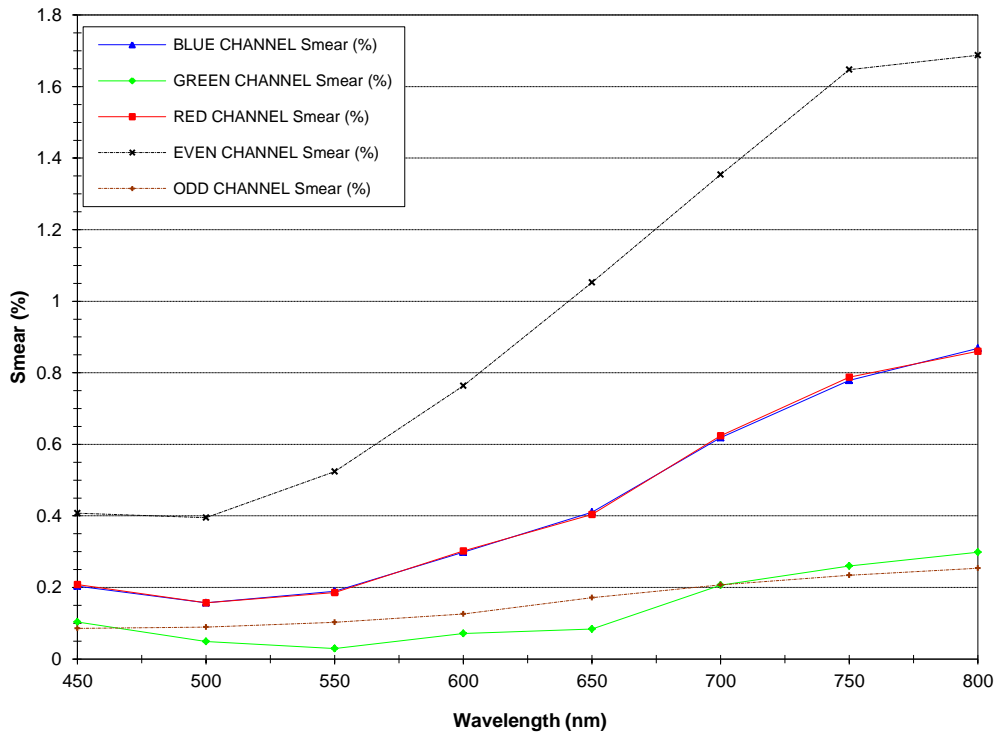


Figure 15: KLI-2104 Smear

**KLI-2104 CTE vs. Frequency**

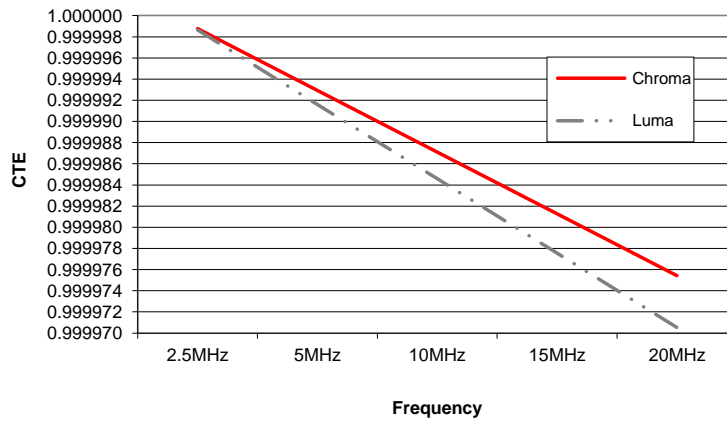


Figure 16: CTE vs. Frequency



Typical KLI-2104 Dark Noise Vs. CCD clock frequency

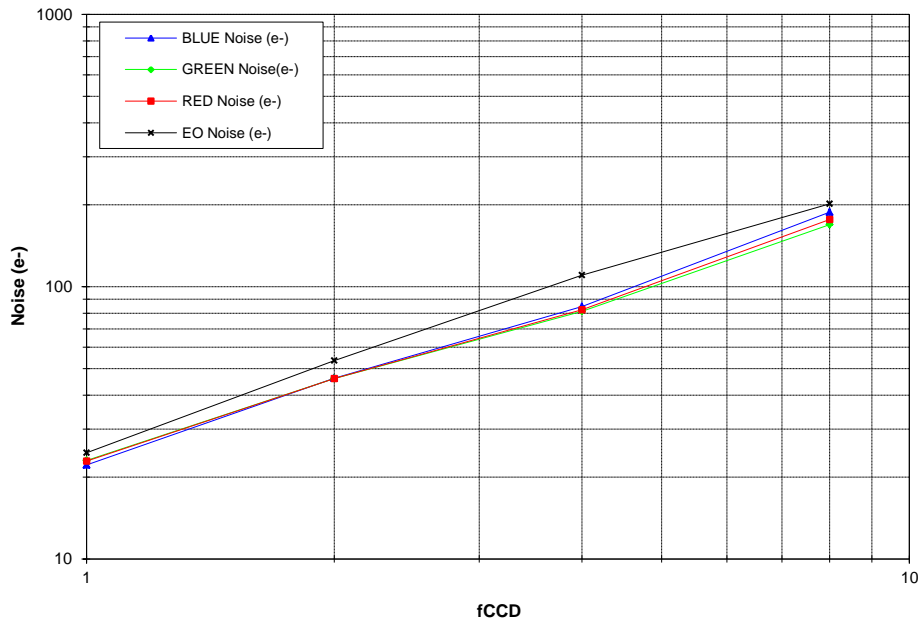


Figure 17: Typical KLI-2104 Dark Noise vs. CCD Clock Frequency

Typical KLI-214 Dark Noise Vs. CCD clock frequency

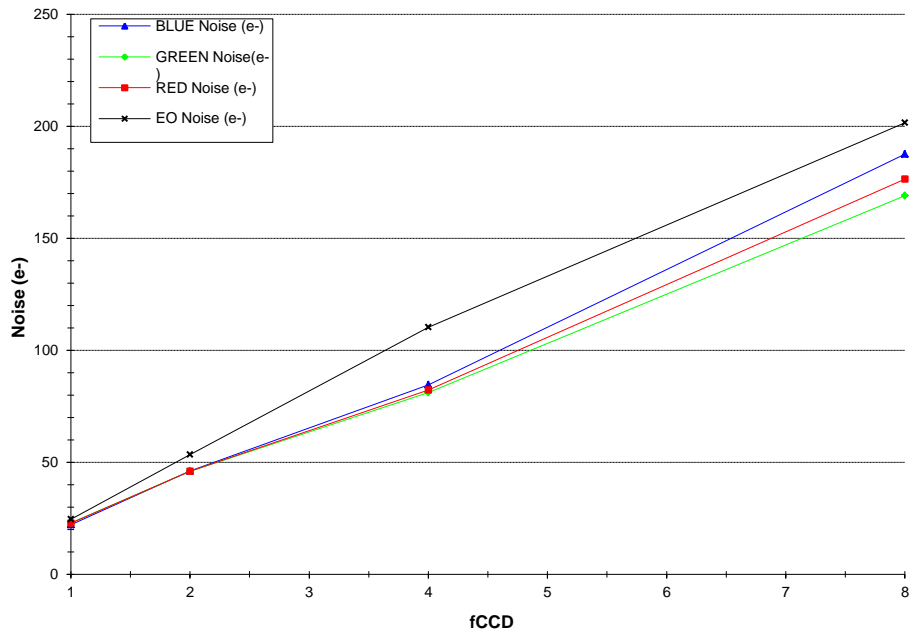


Figure 18: Typical KLI-214 Dark Noise vs. CCD Clock Frequency



Typical KLI-2104 Noise vs Temperature  
1 MHz

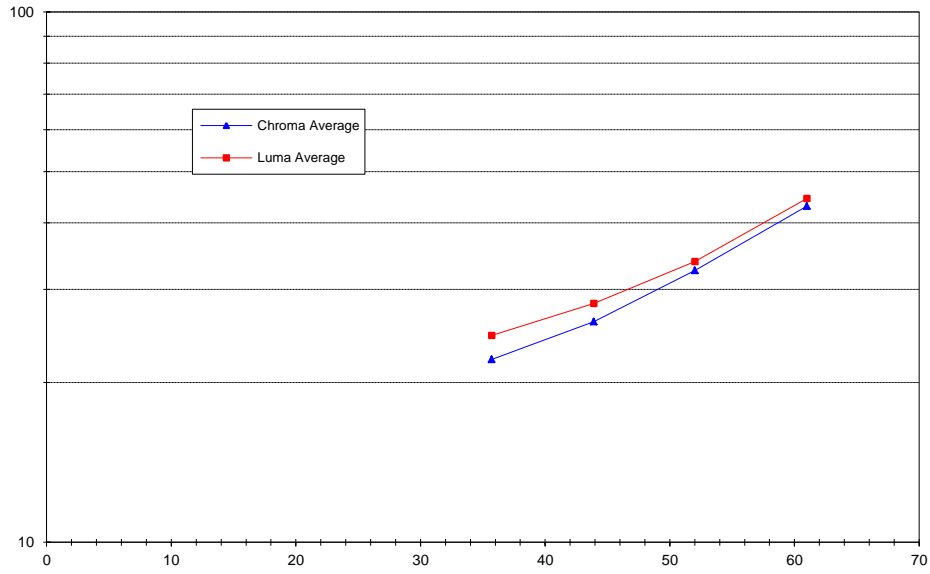


Figure 19: Noise vs. Temperature

Typical KLI-2104 Dark Voltage Vs. Temperature  
1 MHz / Tint = 2.2 ms

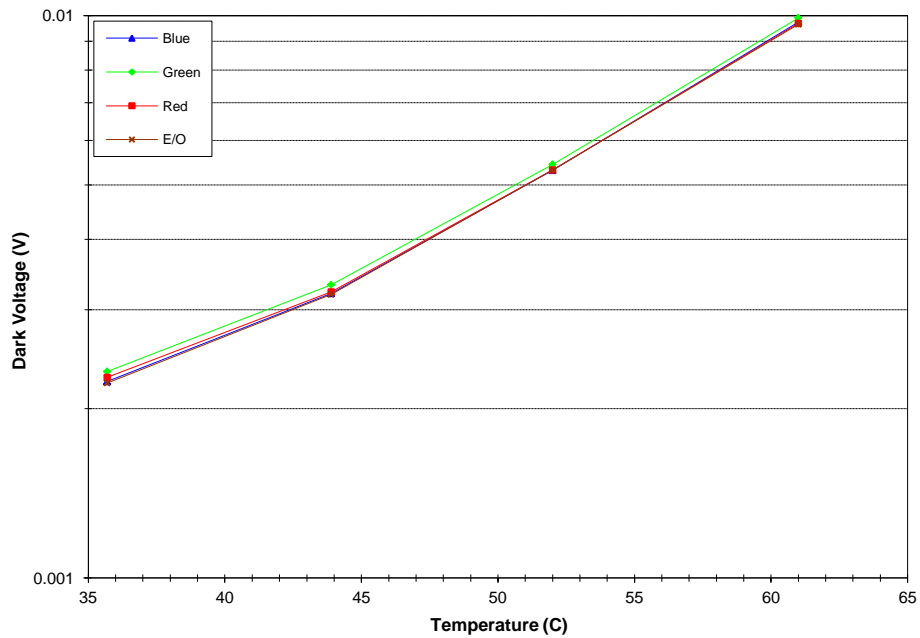


Figure 20: Dark Voltage vs. Temperature



## Operation

### ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Gate Pin Voltages	V <sub>Gate</sub>	0	16	V	1, 2
Pin-to-Pin Voltage	V <sub>Pin-Pin</sub>		16	V	1, 3
Diode Pin Voltages	V <sub>Diode</sub>	-0.5	16	V	1, 4
Output Bias Current	I <sub>DD</sub>	-10	-1	mA	5
Output Load Capacitance	C <sub>VID,Load</sub>		10	pF	9
CCD Clocking Frequency	f <sub>CLK</sub>		20	MHz	6
Operating Temperature	T <sub>OP</sub>	0	70	°C	7
Storage Temperature	T <sub>ST</sub>	-25	80	°C	8

#### Notes:

1. Referenced to substrate voltage.
2. Includes pins: H1n, H2n, TGx, φRx, OGx, IGx.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, VSSn, RDx, VDDx, LS and IDx.
5. Care must be taken not to short output pins to ground during operation as this may cause permanent damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the maximum clocking frequency. VIDn load resistor values may need to be decreased as well.
7. Noise performance will degrade with increasing temperatures.
8. Long term storage at the maximum temperature will accelerate color filter degradation.
9. Exceeding the upper limit on output load capacitance will greatly reduce the output frequency response. Thus, direct probing of the output pins with conventional oscilloscope probes is not recommended.
10. The absolute maximum ratings for the entire table indicate the limits of this device beyond which damage may occur. The Operating ratings indicate the conditions that the device is functional. Operating at or near these ratings do not guarantee specific performance limits. Guaranteed specifications and test conditions are contained in the Imaging Performance section.



### DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Substrate	VSUB C,L	----	0	----	V	
Reset Drain Bias (Color)	VRD C,L	11.5	12	12.5	V	
Output Buffer Supply	VDD C,L	11.5	12	12.5	V	
Output Bias Current/Ch.	$I_{VIDPIN}$	-4	-6	-8	mA	1
Light Shield / Drain Bias	VLS	11.5	12	12.5	V	
Test Pin - Input Gate	VIG C,L	----	0	----	V	
Test Pin - Input Diode	VID C,L	----	12	----	V	

Notes:

1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. The values of  $R_x$  and  $R_L$  should be chosen to optimize for a given operating frequency, but.  $R_x$  should not be less than 75 Ohms. The values shown in Figure 21 below represent one possible solution.

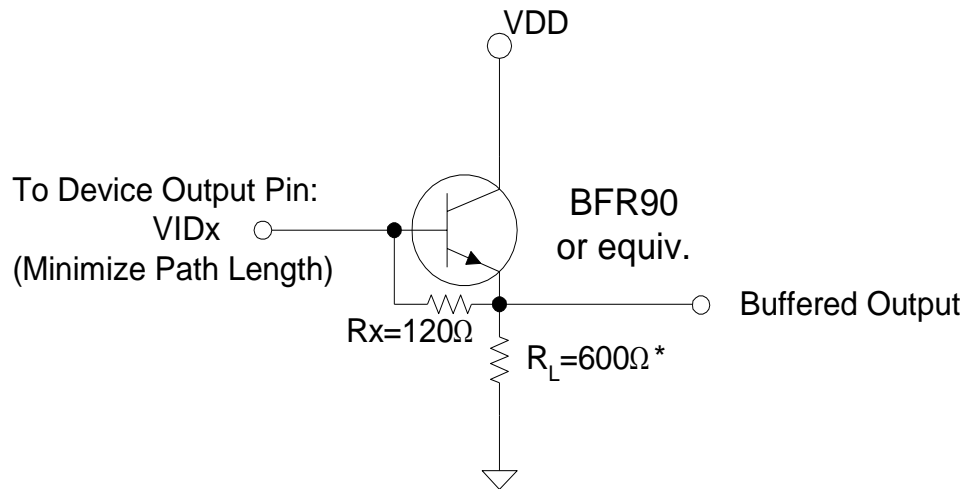


Figure 21: Typical Output Bias/Buffer Circuit



## DEVICE INPUT ESD PROTECTION CIRCUIT (SCHEMATIC)

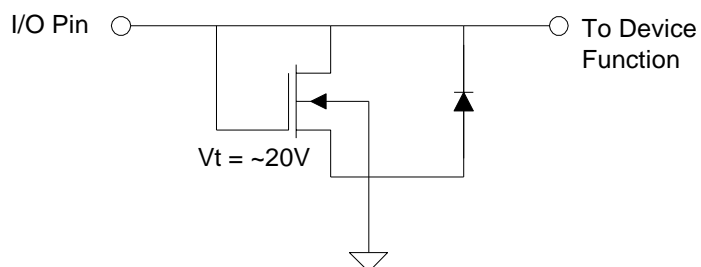


Figure 22: ESD Protection Circuit.

### Caution:

To allow for maximum performance, this device was designed with limited input protection; thus, it is sensitive to electrostatic induced damage. These devices should be installed in accordance with strict ESD handling procedures!



## AC OPERATING CONDITIONS

### AC Electrical Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Element Duration	$1e = 1/f_{CLK}$	50	1000	--	ns	1 e count
$\phi 1L, \phi 1C, \phi 2L, \phi 2C$ , Rise Time	$t_r$	---	30	--	ns	typical
Line/Integration Period	$1L = tint$	0.1064	2.128	--	ms	2128 e counts
PD-CCD Transfer Period	$t_{pd}$	1000	---	--	ns	8 e counts
Transfer Gate 1 Clear	$t_{tg1}$	500	1000	--	ns	1 e count
Transfer Gate 2 Clear	$t_{tg2}$	500	1000	--	ns	1 e count
Reset Pulse Duration	$t_{rst}$	9	--	--	ns	1
Clamp to $\phi 2$ Delay	$t_{cd}$	5	--	--	ns	2
Sample to Reset Edge Delay	$t_{sd}$	5	--	--	ns	2
LOG Gate Duration	$t_{LOG1}$	1000	--	--	ns	
LOG Gate Clear	$t_{LOG2}$	1000	--	--	ns	

#### Notes:

1. Minimum values given are for 20 MHz CCD operation.
2. Recommended delays for Correlated Double Sampling (CDS) of output.

### Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units
CCD Readout Clocks High	$V\phi 1CH, V\phi 2CH, V\phi 1LH, V\phi 2LH$	4.6	5.0	---	V
CCD Readout Clocks Low	$V\phi 1CL, V\phi 2CL, V\phi 1LL, V\phi 2LL$	-0.1	0.0	0.1	V
Transfer Clocks High	$VTGLH, VTG1H, VTG2H$	4.6	5.0	---	V
Transfer Clocks Low	$VTGLL, VTG1L, VTG2L$	-0.1	0.0	0.1	V
Reset Clock High	$V\phi RCH, V\phi RLH$	4.6	5.0	---	V
Reset Clock Low	$V\phi RCL, V\phi RLL$	-0.1	0.0	0.1	V

#### Notes:

1. Care should be taken to insure that low rail overshoot does not exceed -0.5 VDC. Exceeding this value may result in non-photogenerated charged being injected into the video signal.
2. Connect pin to ground potential for applications where exposure control is not required.



## Timing

### REQUIREMENTS AND CHARACTERISTICS

#### Clock Line Capacitance, Chroma

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Phase 1 Clock Capacitance	C $\phi$ 1, C	--	758	--	pF	1
Phase 2 Clock Capacitance	C $\phi$ 2, C	--	558	--	pF	1
Transfer Gate 1 Capacitance	CTG1, C	--	440	--	pF	
Transfer Gate 2 Capacitance	CTG2, C	--	222	--	pF	
Reset Gate Capacitance	C $\phi$ R, C	--	6	--	pF	

#### Clock Line Capacitance, Luma

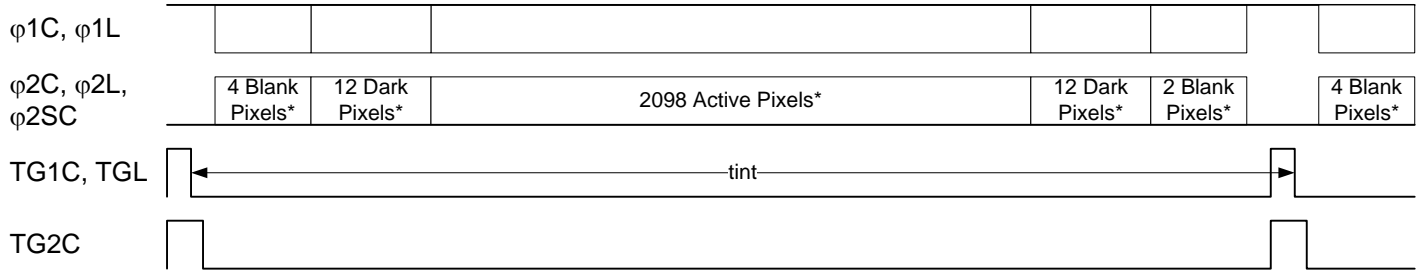
Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Phase 1 Clock Capacitance	C $\phi$ 1, L	--	397	--	pF	1
Phase 2 Clock Capacitance	C $\phi$ 2, L	--	302	--	pF	1
Transfer Gate 1 Capacitance	CTG, L	--	92	--	pF	
Reset Gate Capacitance	C $\phi$ R, L	--	6	--	pF	

#### Notes:

1. This is the total load capacitance per CCD phase. Since the CCDs are driven from both ends of the sensor, the effective load capacitance per drive pin is approximately half the value listed.



**Line Timing - Full Resolution Mode**



\* pixel counts are per output

**Transfer Timing - Full Resolution Mode**

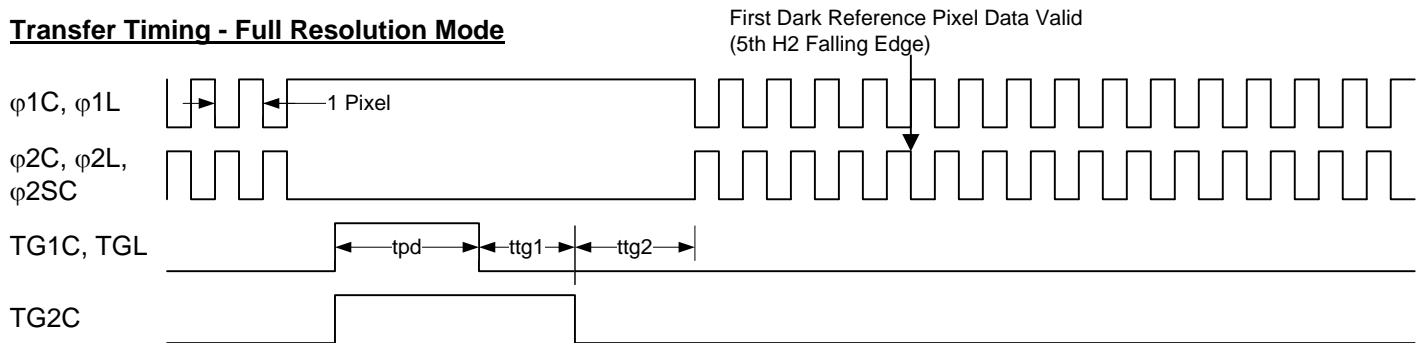
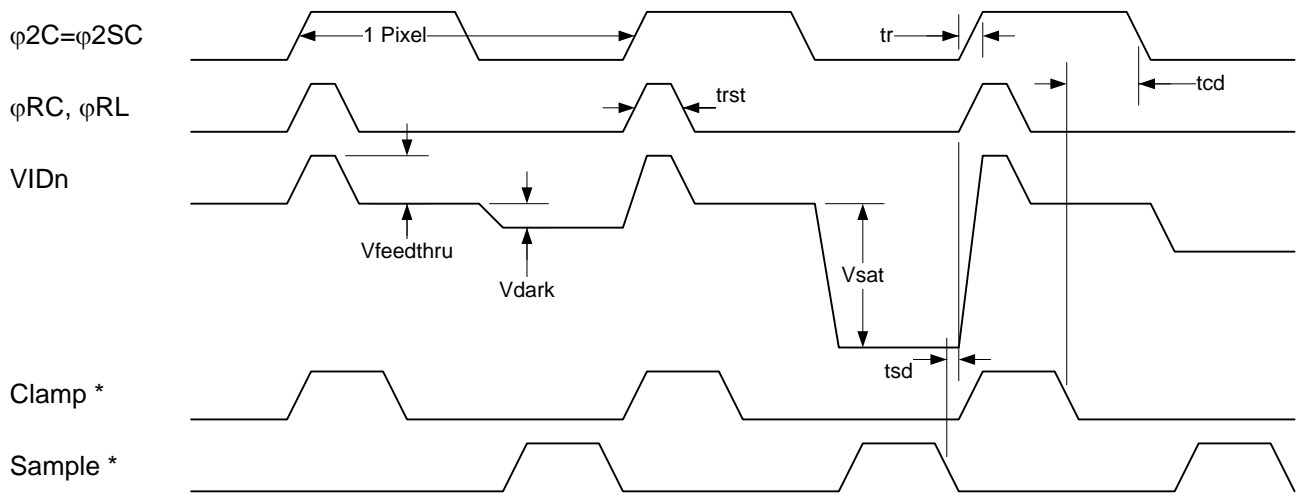


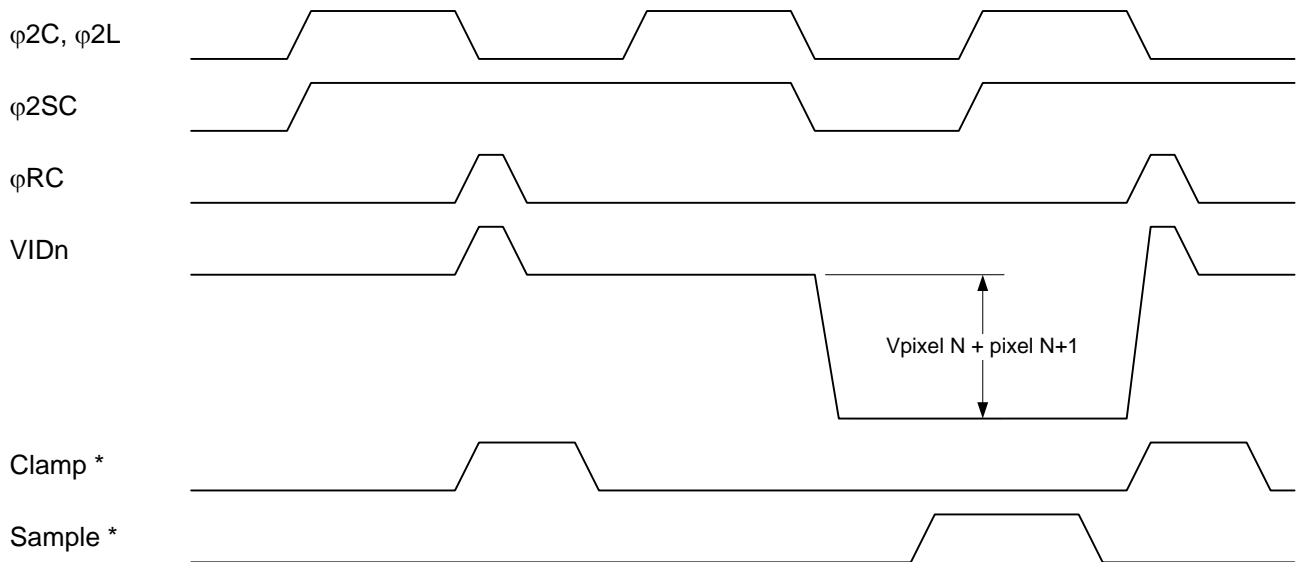
Figure 23: Timing Diagram



**Output Timing (Full Resolution Mode)**



**Output Timing (2-Pixel Summing Mode)**



\* Required for Optional Off-Chip, Analog, Correlated Double Sampling (CDS) Signal Processing

Figure 24: Output Timing



## Storage and Handling

### STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T <sub>ST</sub>	0	70	°C	1
Operating Temperature	T <sub>OP</sub>	-25	+80	°C	2

#### Notes:

- Noise performance will degrade with increasing temperatures.
- Long term storage at these temperatures will accelerate color filter degradation.

### ESD

- This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
- Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
- See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
- Store devices in containers made of electro-conductive materials.

### COVER GLASS CARE AND CLEANLINESS

- The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
- Touching the cover glass must be avoided.

- Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

### ENVIRONMENTAL EXPOSURE

- Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
- Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
- Avoid sudden temperature changes.
- Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
- Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

### SOLDERING RECOMMENDATIONS

- The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
- Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.



## Mechanical Drawings

### COMPLETED ASSEMBLY

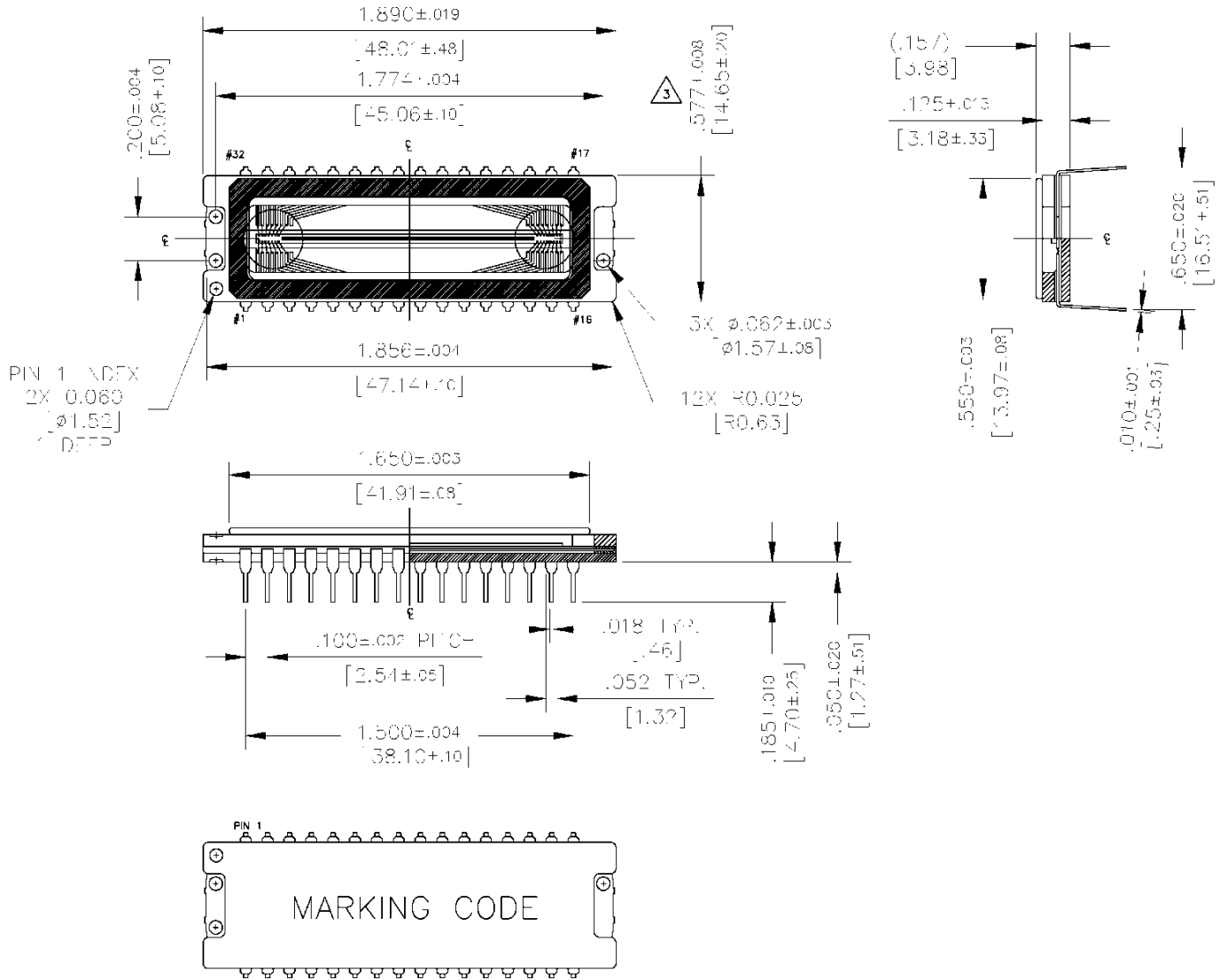


Figure 25: Completed Assembly



## Cover Glass Specification

### TWO-SIDED MULTI-LAYER ANTI-REFLECTIVE COVER GLASS SPECIFICATION (MAR)

This device is configured with a coverglass designed to reduce reflections and maximize transmission of the visible light. The typical spectral characteristics of this glass is found below:

#### Maximum Reflectance Allowed (two sided)

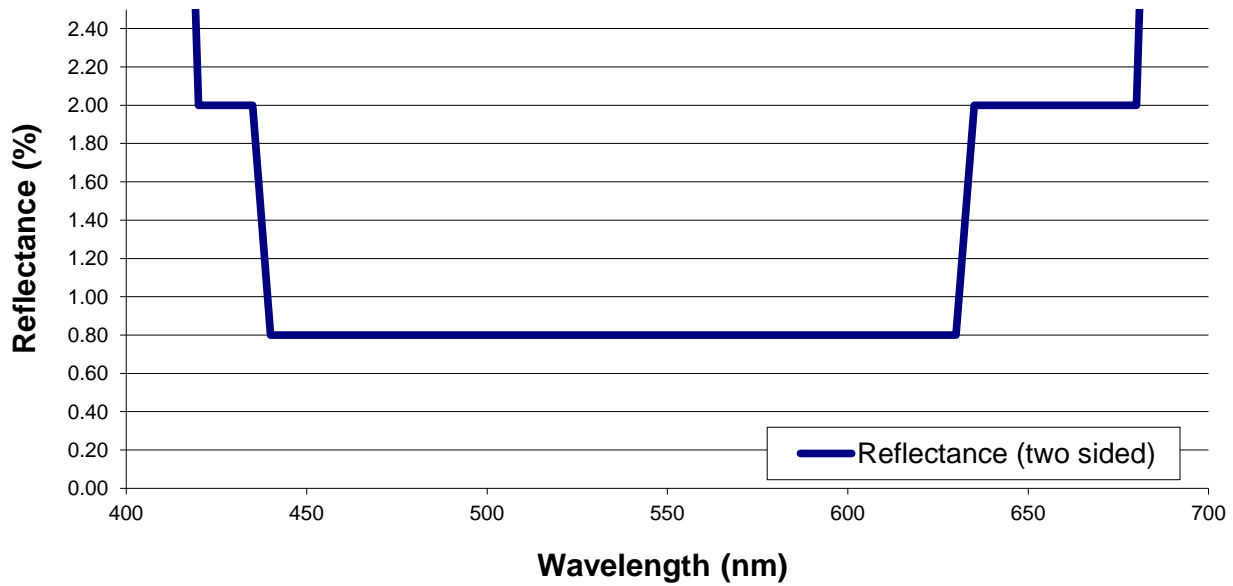


Figure 26: Maximum Reflectance Allowed





## Quality Assurance and Reliability

### QUALITY AND RELIABILITY

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

### REPLACEMENT

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

### LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

### LIABILITY OF THE CUSTOMER

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

### TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

### MECHANICAL

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

## Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.




## Revision Changes

### MTD/PS-0212

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> <li>Initial Release</li> </ul>
2.0	<ul style="list-style-type: none"> <li>Confirmed Filter Variation Parameters for Filter Group II Color image Sensors. (Page 8)</li> <li>Confirmed Luminance Channel Responsivity. (Page 9)</li> <li>Confirmed Typical Performance Measurements for Quantum Efficiency for Monochrome and Color Channels. (Page 17)</li> </ul>
3.0	<ul style="list-style-type: none"> <li>Update to Summary Specification description and formatting</li> </ul>
4.0	<ul style="list-style-type: none"> <li>Update to Summary Specification description, performance tables, and Quality Assurance and Reliability page.</li> </ul>

### PS-0049

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> <li>Initial release with new document number, updated branding and document template</li> <li>Updated <i>Storage and Handling</i> and <i>Quality Assurance and Reliability</i> sections</li> </ul>
1.1	<ul style="list-style-type: none"> <li>Updated branding</li> </ul>

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